Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently Amended) An accelerated graphics processing subsystem comprising: a graphics command replicator; a plurality of [[off-the-shelf]] video cards; a mechanism to synchronize the signal by said plurality of video cards; and a video merger hub,

wherein said mechanism to synchronize the signal operates on the basis of: the vertical refresh rate of said output signals from said plurality of video cards; the vertical resolution of said output signals from said plurality of video cards; and the load balancing ratio assigned to each of said plurality of video cards.

Claim 2. (Original) The accelerated graphics processing subsystem of claim 1 wherein: said graphics command replicator is a software module that intercepts graphics commands issued by an application and generates multiple, modified graphics command streams; the number of said multiple, modified graphics command streams is equal to the number of said plurality of video cards; and each of said multiple, modified graphics command streams is received by a separate video card selected from said plurality of video cards.

Claim 3. (Original) The accelerated graphics processing subsystem of Claim 2 wherein said graphics command replicator generates said multiple, modified graphics command streams such that each of said multiple, modified graphics command streams contains commands to draw only a portion of a graphics screen.

Claim 4. (Original) The accelerated graphics processing subsystem of Claim 3 wherein the output signals from said plurality of video cards is combined into a single graphics output signal by said video merger hub and is displayed on a visual output device.

Claim 5. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[4]] wherein said visual output device is an output device selected from the group consisting of: cathode ray tube displays, liquid crystal displays, plasma screen displays, projection displays, OLED displays, head-mounted displays and hybrids thereof.

Claim 6. (Original) The accelerated graphics processing subsystem of claim 2 wherein said intercepted graphics commands are API commands and said multiple, modified graphics command streams are multiple, modified API command streams.

Claim 7. (Original) The accelerated graphics processing subsystem of claim 6 wherein said multiple, modified API command streams are each received by a separate instance of an API module and wherein each of said API module instances generates a command stream which is processed by a separate video card selected from said plurality of video cards.

Claim 8. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[4]] wherein said modifications to said multiple, modified graphics command streams are accomplished by incorporating therein a clipping command.

Claim 9. (Original) The accelerated graphics processing subsystem of claim 8 wherein said clipping command is a 2D clipping command.

Claim 10. (Original) The accelerated graphics processing subsystem of claim 8 wherein said clipping command is a 3D clipping command.

Claim 11. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[4]] wherein the sum of all said portions of said graphics screen combine to generate a full graphics screen.

Claim 12. (Original) The accelerated graphics processing subsystem of claim 11 wherein said portions of said graphics screen are non-overlapping.

Claim 13. (Original) The accelerated graphics processing subsystem of claim 11 wherein said portions of said graphics screen have overlapping regions.

Claim 14. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[4]] wherein the sum of all said portions of said graphics screen combine to generate a partial graphics screen.

Claim 15. (Original) The accelerated graphics processing subsystem of claim 14 wherein said portions of said graphics screen are non-overlapping.

Claim 16. (Original) The accelerated graphics processing subsystem of claim 14 wherein said portions of said graphics screen have overlapping regions.

Claim 17. (Original) The accelerated graphics processing subsystem of claim 4 wherein each of said plurality of video cards is equipped with a single GPU.

Claim 18. (Original) The accelerated graphics processing subsystem of claim 4 wherein each of said plurality of video cards is equipped with a plurality of GPUs.

Claim 19. (Original) The accelerated graphics processing subsystem of claim 4 wherein said plurality of video cards is comprised of a combination of video cards equipped with a plurality of GPUs and video cards equipped with a single GPU.

Claim 20. (Original) The accelerated graphics processing subsystem of claim 4 wherein said mechanism to synchronize the signal output by said plurality of video cards is a genlock mechanism.

Claim 21. (Original) The accelerated graphics processing subsystem of claim 4 wherein said mechanism to synchronize the signal output by said plurality of video cards consists of

designating the timing regulating device in one of said plurality of video cards as a master timing regulating device and designating timing regulating devices in the remainder of said plurality of video cards as slaves of said master timing regulating device.

Claim 22. (Original) The accelerated graphics processing subsystem of claim 21 wherein the timing reference sources for said master and slave timing regulating devices are timing reference sources selected from the group consisting of piezoelectric crystals, programmable crystals, oscillators, programmable oscillators and combinations thereof.

Claim 23. (Original) The accelerated graphics processing subsystem of Claim 4 wherein said video merger hub is comprised of:

a video switch;

a video switch controller;

a microcontroller; and

a video output.

Claim 24. (Original) The accelerated graphics processing subsystem of Claim 23 wherein said video switch receives said output signals from said plurality of video cards and sequentially routes selected portions of said output signals from said plurality of video cards to said video output.

Claim 25. (Original) The accelerated graphics processing subsystem of Claim 24 wherein said video switch is controlled by said video switch controller.

Claim 26. (Original) The accelerated graphics processing subsystem of Claim 25 wherein said video switch controller controls said video switch by triggering routing switches at appropriate intervals.

Claim 27. (Original) The accelerated graphics processing subsystem of Claim 26 wherein said routing switch triggering intervals are determined on the basis of:

the vertical refresh rate of said output signals from said plurality of video cards;

the vertical resolution of said output signals from said plurality of video cards; and

the load balancing ratio assigned to each of said plurality of video cards.

Claim 28. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[27]] wherein said load balancing ratio is transmitted by said microcontroller to said video switch controller.

Claim 29. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[27]] wherein said load balancing ratio is assigned by a user through software.

Claim 30. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[27]] wherein said load balancing ratio is equal for each of said video cards.

Claim 31. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[27]] wherein said load balancing ratio is based on each of said video cards' graphics throughput.

Claim 32. (Currently Amended) The accelerated graphics processing subsystem of claim 1 [[27]] wherein said load balancing ratio is dynamically adjusted to maximize the throughput of said subsystem by utilizing a test feedback loop program which measures the load on each of said video cards and makes appropriate adjustments.

Claims 33 -64 (Cancelled)

Claim 65. (Original) An accelerated graphics processing subsystem comprising: a graphics command replicator consisting of a software module that intercepts graphics commands issued by an application and generates multiple, modified graphics command streams; a plurality of

video cards, each equipped with one or more GPUs, wherein the number of said multiple, modified graphics command streams is equal to the number of said plurality of video cards; a mechanism to synchronize the signal output by said plurality of video cards; and a video merger hub comprised of a video switch, a video switch controller, a microcontroller, and a video output; wherein said graphics command replicator generates said multiple, modified graphics command streams such that each of said multiple, modified graphics command streams contains commands to draw only a portion of a graphics screen; each of said multiple, modified graphics command streams is received by a separate video graphics card selected from said plurality of video cards; output signals from said plurality of video cards are received by said video switch and selected portions thereof are sequentially routed to said video output and displayed on a visual output device; and said video switch is controlled by said video switch controller through the triggering of routing switches at appropriate intervals determined by the vertical refresh rate and vertical resolution of said output signals from said plurality of video cards and by the load balancing ratio assigned to each of said plurality of video cards.

Claim 66. (Original) A method for accelerating the processing of graphics instructions on a computer through use of a plurality of video cards, comprising the steps of: intercepting graphics commands issued by an application and generating multiple, modified graphics command streams wherein the number of said multiple, modified graphics command streams is equal to the number of said plurality of video cards; synchronizing the signal output by said plurality of video cards; combining the output signal from said plurality of video cards into a single graphics output signal through use of a video merger hub comprised of a video switch, a video switch controller, a microcontroller, and a video output; and displaying said single graphics output signal on a visual output device; wherein each of said multiple, modified graphics command streams contains commands to draw only a portion of a graphics screen; each of said multiple, modified graphics command streams is received by a separate video graphics card selected from said plurality of video cards; output signals from said plurality of video cards are received by said video switch and selected portions thereof are sequentially routed to said video output and displayed on a visual output device; and said video switch is controlled by said video switch controller through the triggering of routing switches at appropriate intervals determined by the

vertical refresh rate and vertical resolution of said output signals from said plurality of video cards and by the load balancing ratio assigned to each of said plurality of video cards.

Claim 67. (Currently Amended) A video merger hub for combining the output signals from a plurality of video cards into a single graphics output signal displaying said single graphics output signal on a visual output device comprised of: a video switch; a video switch controller; a microcontroller; and a video output,

wherein said video switch receives said output signals from said plurality of video cards and sequentially routes selected portions of said output signals from said plurality of video cards to said video output,

wherein said video switch is controlled by said video switch controller,

wherein said video switch controller controls said video switch by triggering routing switches at appropriate intervals, and

wherein said routing switch triggering intervals are determined on the basis of: the vertical refresh rate of said output signals from said plurality of video cards; the vertical resolution of said output signals from said plurality of video cards; and the load balancing ratio assigned to each of said plurality of video cards.

Claims 68-71 (cancelled)

Claim 72. (Currently Amended) The video merger hub of claim 67 [[71]] wherein said load balancing ratio is transmitted by said microcontroller to said video switch controller.

Claim 73. (Currently Amended) The video merger hub of claim 67 [[71]] wherein said load balancing ratio is assigned by a user through software.

Claim 74. (Currently Amended) The video merger hub of claim 67 [[71]] wherein said load balancing ratio is equal for each of said video cards.

Claim 75. (Currently Amended) The video merger hub of claim 67 [[71]] wherein said load balancing ratio is calculated by determining an optimized load balancing ration for each of said video cards based on its graphics throughput.

Claim 76. The video merger hub of claim 71 wherein said load balancing ratio is dynamically adjusted to maximize the throughput of said subsystem by utilizing a test feedback loop program which measures the load on each of said video cards and makes appropriate adjustments.